

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1 - 10 (canceled):

- 1 **Claim 11 (previously presented):** A semiconducting structure having reduced with soft
2 error rates comprising:
3 a semiconductor substrate;
4 a first semiconductor layer over the substrate, said first semiconductor layer being
5 comprised of a first semiconductor material and having a vertical extent defined by an
6 upper extent of the first semiconductor material and a lower extent of the first
7 semiconductor material;
8 a generally constant electric field across at least a portion of the vertical extent of
9 the first semiconductor material, wherein a charge which occurs within the first
10 semiconductor layer is influenced toward the semiconductor substrate; and
11 a device layer in which a semiconductor device may be fabricated.

1 **Claim 12** (previously presented): The semiconducting structure recited in claim 11
2 above, wherein the first semiconductor layer over the substrate further comprises a
3 graded dopant concentration over the at least a portion of the vertical extent of the first
4 semiconductor material, said graded dopant concentration having a first dopant
5 concentration established at the lower extent of the semiconductor material, a second
6 dopant concentration established at the upper extent of the semiconductor material and a
7 plurality of dopant concentrations between said first dopant concentration and said
8 second dopant concentration over the at least a portion of the vertical extent of the first
9 semiconductor material, and between the upper extent and lower extent of the first
10 semiconductor material.

1 **Claim 13** (original): The semiconducting structure recited in claim 12 above, wherein
2 said second dopant concentration is based on said semiconductor device to be fabricated
3 in the device layer.

1 **Claim 14** (original): The semiconducting structure recited in claim 12 above, wherein
2 said device layer is formed within the vertical extent of first semiconductor material.

1 **Claim 15** (original): The semiconducting structure recited in claim 13 above further
2 comprises:

3 a second electric field formed at the lower extent of the first semiconductor
4 material.

1 **Claim 16** (currently amended): The semiconducting structure recited in claim 15 above,
2 wherein the second dopant concentration is further based on a dopant concentration of
3 said semiconductor substrate, wherein said second dopant concentration is different from
4 said dopant concentration of said semiconductor substrate.

1 **Claim 17** (original): The semiconducting structure recited in claim 13 above further
2 comprises:

3 a second electric field below the first semiconductor material.

1 **Claim 18** (original): The semiconducting structure recited in claim 17 above, wherein
2 said semiconductor substrate is a P+ semiconductor substrate, and said semiconducting
3 structure further comprises:

4 an undoped intrinsic layer formed over said P+ semiconductor substrate and under
5 said first semiconductor layer.

1 **Claim 19** (previously presented): The semiconducting structure recited in claim 17
2 above, wherein said semiconductor substrate is a P- semiconductor substrate, and
3 semiconducting structure further comprises:

4 a buried n-layer formed over said P- semiconductor substrate; and

5 an undoped intrinsic layer formed over said buried n-layer and formed under said
6 first semiconductor layer.

1 **Claim 20** (canceled):